forming a low-dielectric layer over the patterning layer;

forming a photoresist pattern whose width is equal to the exposure limit on the low-dielectric layer;

patterning the low-dielectric layer using the photoresist pattern as a mask;

removing the photoresist pattern;

shrinking the low-dielectric pattern; and

forming the fine patterns by patterning the patterning layer using the shrunken low-dielectric pattern as a mask.

8. (Amended) The method of claim 6 or 7, wherein forming the low-dielectric layer comprises:

depositing a low-dielectric layer over the patterning layer for the fine patterns; and

soft-baking the low-dielectric layer at a predetermined temperature.

REMARKS

In the Final Office Action dated December 3, 2002, the Examiner rejected claims 6-10 under 35 U.S.C. § 112, second paragraph and rejected claims 1-10 under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. (U.S. Patent No. 6,080,529) in view of Lau et al. (U.S. Patent No. 5,173,542).

Based on the following remarks, Applicants respectfully traverse the rejections under 35 U.S.C. § 112, second paragraph and 35 U.S.C. §103(a).

Regarding the rejections of claims 6-10 under 35 U.S.C. § 112, second paragraph, Applicants propose to amend claims 6 and 8 by replacing the phrase "material" with the phrase "patterning." Accordingly, claims 6 and 8 now include a "patterning layer" that is formed on a semiconductor wafer. Applicants submit that the proposed amendments to claims 6 and 8 are not made for reasons of patentability

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com